Performance Analysis of Z-Source Inverter Considering Inductor Resistance

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***Abstract*—This paper presents mathematical and experimental analysis of Z-source inverters (ZSI) when feeding inductive loads. A focus has been given to the effect of considering inductors resistance of the inverter. A simple mathematical form has been derived to obtain the voltage transfer ratio (VTR) in terms of inverter and load parameters for different control techniques. Comparison between experimental and calculated results showed acceptable validity for both maximum boost and maximum constant boost control techniques. The obtained analysis and relations are useful in designing and operating Z-source inverters.**

Keywords—Z-source inverters; maximum boost control; maximum constant boost control

I. INTRODUCTION

Nowadays, using renewable energy and distributed generation sources in electric power systems is increasing rapidly. Many of these sources may operate as a low DC voltage source [1]. In order to achieve load requirements or compatibility with power grid, the need for voltage boosting converters became mandatory. Traditional techniques depend upon dc/dc boosting converter followed by a voltage source inverter (VSI). Such systems still have problems such as high cost and complexity associated with two-stage power conversion [2]. Recently, Z-source inverters (ZSI) are used as an alternative to achieve the same goal. Such a type of converter is controlled using pulse width modulation (PWM). This development has been firstly suggested by F. Z. Peng [3] in 2003. The unique feature of the PWM Z-source inverter is that it can be used as a voltage buck-boost inverter while conventional VSI achieve buck operation only. ZSI was applied for different applications such as adjustable speed drive systems [4-5], fuel cell vehicles [6], residential photovoltaic systems [7], wind power generation [8] and traction drive applications [9]. The transient modeling and controller was also investigated in [10] and [11]. In recent years, ZSI has attracted researches to investigate its operation and enhance controller behavior [5]-[12].

In principle, a ZSI consists of a diode, impedance network and a traditional VSI. Impedance network is composed from two identical inductors and two identical capacitors connected in X shape as shown in Fig. 1. Existence of impedance network allows VSI to be operated in a new state called “shoot through state” which is used to get boosting behavior.

Z-source inverters can be controlled using several boosting techniques, e. g. simple boost (SB) [3], maximum boost (MB) [13], maximum constant boost (MCB) [14] and modified space vector pulse width modulation (MSVPWM) [15]. Most of published work neglects the effects of internal inductor resistance that results in inaccurate design and controlled behavior. Hence, the motivation of this work is to investigate the effect of this resistance and determine voltage transfer ratio VTR for ZSI to obtain a simple and closed formula.

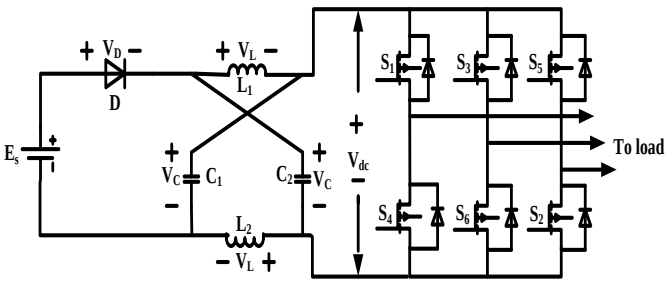


Fig. 1. Three-Phase Z-Source Inverter

Section II presents operation principles for ZSI, the equivalent circuits and the different modulation boosting schemes. Section III explains how output-to-input voltage transfer ratio is determined for two case, ideal system and considering inductor parasitic resistance. In section IV, experimental and simulation results are compared with those obtained using suggested theoretical analysis. Finally conclusions are given in section V.

II. PRINCIPLES OF Z-SOURCE INVERTER AND MODULATION SCHEMES

In a traditional operation of VSI, there are eight switching states, six of them are called “active states" where the load is connected directly to the supply voltage. The remaining two states are named as "null states" where either all upper or all lower switches are conducted simultaneously. The null states achieve zero line voltage across load terminals [16].

For ZSI, there is an additional state called shoot through state. In this state, the dc link terminals are shorted by gating both the upper and lower devices of at least one inverter leg [1]. There are seven different ways to generate shoot-through states, three of them can be achieved by shorting any one phase leg. Other three ways are obtained by shorting any two phase legs simultaneously. The last way is obtained by shorting three phase legs simultaneously. Both null and shoot through states achieve zero load voltage but the main difference is that, shoot through facilitates boosting of dc link voltage through the impedance network.

When using any technique of SB, MB and MCB, the PWM switching pattern for a ZSI can be generated according to the following switching manner. Both active and null states are generated using traditional sinusoidal pulse width modulation (SPWM) technique. The shoot-through states are generated by comparing other modulating signals with the employed triangular carrier signal. The shoot-through states are distributed within the null states, so that active states intervals aren't affected. Fig .2 shows the sketch map of SB, MB and MCB boosting techniques.

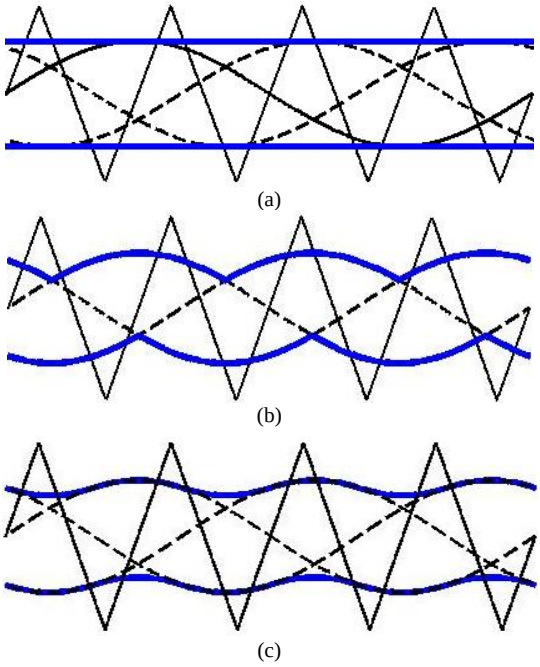


Fig. 2. Modulation schemes (a) SB, (b) MB and (c) MCB

III. OUTPUT-TO-INPUT VOLTAGE TRANSFER RATIO

Output-to-input voltage transfer ratio is defined as the ratio between inverter output peak phase voltage to the dc supply voltage. This ratio has been obtained for two cases. The First case is when neglecting the parasitic resistances of all components (diode, inductors, capacitors, MOSFETs…etc). In the second case: the effect of the inductor resistance "r" is considered while setting all components in ideal case.

As described in [1], there are two available states of operation. The first is shoot through state which has the equivalent circuit shown in Fig. 3.a. This state begins when the Z-source network is shorted by any of the seven shoot through states for an interval of T_{sh}. In this state, the sum of two capacitor voltages is greater than the source voltage E_s, so that the diode is reverse biased with voltage V_D. Hence, the stored energy in the capacitors is transferred to inductors, thereby achieving the boosting of the voltage applied to the VSI. The second case is non shoot through state (either active or null state). The equivalent circuit of is shown in Fig 3.b. the ZSI operates in one of the six active and two null states for total interval of T_{an}. In this state, the diode is forward biased. So, the capacitors begin to charge and the energy that initially stored in the inductors will be transferred to the load.

A. Ideal Case

The analysis of ideal case can be performed by setting *r=0* in equivalent circuit of Fig. 3

A. 1. Shoot-through state $0 \le t \le T_{sh}$

From the equivalent circuit:

$$V_L = V_C \quad (1)$$

$$V_{dc} = 0 \quad (2)$$

$$V_D = E_s - 2V_C \quad (3)$$

A. 2. Non shoot-through state $T_{sh} \le t \le T$

According to the equivalent circuit given in Fig 3.b

$$V_L = E_S - V_C \quad (4)$$

$$V_{dc} = V_C - V_L \quad (5)$$

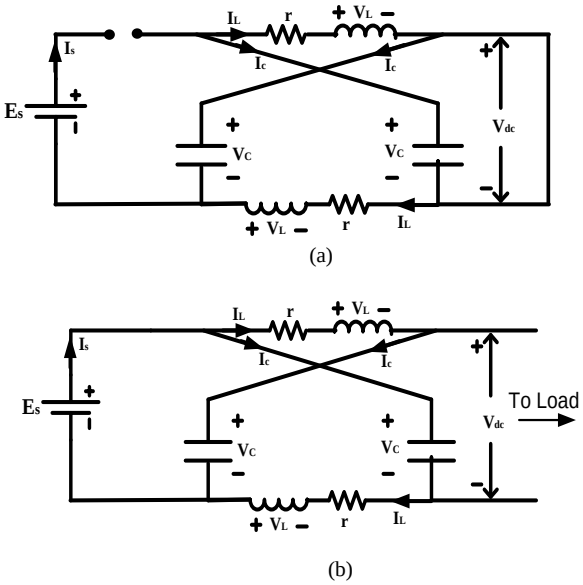


Fig. 3. Equivalent circuit of the Z-source inverter (a) Shoot–through state (b) Non shoot–through state.

Substituting from (4) into (5) for V_L results in:

$$V_{dc} = 2V_C - E_S \quad (6)$$

At steady state, the average value of the inductor voltage over one switching period equals zero [1], V_C can be assumed constant within the time T_{sh}, by using (1) and (4):

$$\frac{1}{T}\int_0^T V_L(t)\,dt = \frac{1}{T}\left[\int_0^{T_{sh}} (V_c)\,dt + \int_{T_{sh}}^{T} (E_S - V_c)\,dt\right] = 0 \quad (7)$$

from which, the average capacitor voltage is given by:

$$V_c = \frac{T_{an}}{T_{an} - T_{sh}} E_S \quad (8)$$

where T_{sh}, T_{an} is the shoot through and non shoot through periods respectively. T is switching period where:

$$T = T_{sh} + T_{an} \quad (9)$$

Let D_{sh} and D_{az} are the shoot through and non shoot through duty ratios respectively where:

$$D_{sh} = \frac{T_{sh}}{T} \quad (10)$$

$$D_{an} = \frac{T_{an}}{T} \quad (11)$$

From (8), (9), (10) and (11), the average capacitor voltage is given by:

$$V_c = \frac{1 - D_{sh}}{1 - 2D_{sh}} E_S \quad (12)$$

Substituting from (12) into (6) for V_c, the peak dc-link voltage across inverter terminals is given by:

$$V_{dc\,(peak)} = \frac{1}{1 - 2D_{sh}} E_S \quad (13)$$

Let boost factor B is defined as follows:

$$B = \frac{1}{1 - 2D_{sh}} \quad (14)$$

For stable operation, D_{sh} is in the range between zero and 0.5. Therefore, B varies from one to infinity. Practically, values of B are affected by source of non idealities such as internal resistance of inductance. The peak of the fundamental output phase voltage (V_m) can be expressed in terms of peak dc link voltage and modulation index M as follows [2]:

$$V_m = M\,\frac{V_{dc\,(peak)}}{2} \quad (15)$$

Substituting from (13) and (14) into (15), results in:

$$V_m = \frac{G}{2} E_S \quad (16)$$

where $G = MB$ is the ZSI gain [1]. In ZSI, voltage transfer ratio V_m / E_S is similar to that of VSI but multiplied by boost factor (B).

According to [3-5], a general form for modulation index M as a function of duty ratio D_{sh} can be put in the following form:

$$M = \frac{2}{n}(1 - D_{sh}) \quad (17)$$

Similarly, the general form for gain G as a function of modulation index M is obtained as follows:

$$G = \frac{M}{nM - 1} \quad (18)$$

where n depends on the employed modulation technique as given by the following table:

TABLE I. VALUES OF PARAMETER "N" FOR DIFFERENT MODULATION TECHNIQUES

Modulation technique	SB	MB & MSVPWM	CB
n	**2**	$\mathbf{3\sqrt{3}/\pi}$	$\mathbf{\sqrt{3}}$

From (16) voltage transfer ratio VTR can be defined as follows for r=0:

$$VTR = \frac{G}{2} \quad (19)$$

B. Considering Inductor Resistance

Practically, all components (such as inverter switches, diode, inductors and capacitors) have internal parasitic resistances. The inductor resistance has a major effect because it carries higher current levels compared with other components. In this section, ZSI steady state analysis is given when considering inductor parasitic resistance "r" connected in series.

B. 1. Shoot-through state $0 \le t \le T_{sh}$

The equivalent circuit for this state is shown in Fig. 3.a. From which the following equations can be written:

$$V_L = V_C - r\,I_L \quad (20)$$

$$V_{dc} = 0 \quad (21)$$

B. 2. Non shoot-through state $T_{sh} \le t \le T$

The equivalent circuit of this state is shown in Fig. 3.b. From which the following equations can be written:

$$V_L = E_S - V_C - r\,I_L \quad (22)$$

$$V_{dc} = V_C - V_L - r\,I_L \quad (23)$$

Substituting from (22) into (23) for V_L results in:

$$V_{dc} = 2V_C - E_S \quad (24)$$

At steady state, the average value of the inductor voltage over one switching period equals zero [1]. Using (20) and (22), the average capacitor voltage is given by:

$$V_c = \frac{1 - D_{sh}}{1 - 2D_{sh}} E_S - \frac{1}{1 - 2D_{sh}} r\, I_L \tag{25}$$

Substituting from (25) into (24) for V_c, the peak dc-link voltage across inverter terminals over a switching period is given by:

$$V_{dc\,(peak)} = \frac{1}{1 - 2D_{sh}} E_S - \frac{2}{1 - 2D_{sh}} r I_L \tag{26}$$

substituting from (26) into (15), the fundamental peak of output phase voltage can be obtained as follows:

$$V_m = \frac{G}{2}\,(E_S - 2rI_L) \tag{27}$$

Inductor current I_L can be calculated from power balance equation as follows:

$$P_o = P_s - 2P_{loss} \tag{28}$$

where

$$P_o = \frac{3}{2} V_m I_m \cos(\Phi) \tag{29}$$

P_o is the load power, Φ is load power factor angle, P_s is the average source power and P_{loss} is the inductor power loss Equation (29) can be written in the following form:

$$P_o = \frac{3}{2} \frac{V_m{}^2 \cos(\Phi)}{Z_L} \tag{30}$$

where

$I_m = \frac{V_m}{Z_L}$ and Z_L is the load impedance

The average source power and inductor power loss are given by:

$$P_s = E_S I_S \tag{31}$$

$$P_{loss} = r I_L{}^2 \tag{32}$$

Since, the average capacitor current is zero, the average inductor current I_L equals average supply current I_S. Therefore From (28) to (32), inductor current is given by:

$$I_L = \frac{E_s - \sqrt{E_S{}^2 - \frac{12rcos(\Phi)V_P{}^2}{Z_L}}}{4r} \tag{33}$$

Substituting from (33) into (26), the peak value of dc link voltage (stress voltage V_s) is given by:

$$V_{dc\,(peak)} = \frac{4(nG - 1)}{4 + \frac{12rcos(\Phi)}{Z_L}(nG - 1)^2} E_S \tag{34}$$

Substituting from (33) into (27), the fundamental peak of output phase voltage is:

$$V_m = \frac{16G}{16 + \frac{12rcos(\Phi)}{Z_L} G^2} \frac{E_S}{2} \tag{35}$$

Equation (35) can be written in the following form:

$$V_m = G_n \frac{E_S}{2} \tag{36}$$

where

$$G_n = \frac{16G}{16 + \frac{12rcos(\Phi)}{Z_L} G^2} \tag{37}$$

where G_n is ZSI gain when considering inductor resistance.

The output to input voltage transfer ratio (V_m/E_S) is given by:

$$VTR = \frac{8G}{16 + \frac{12rcos(\Phi)}{Z_L} G^2} \tag{38}$$

It is to be noted that, if the inductor resistance (r) approaches zero, equation (38) tends to (19). It is obvious that, VTR depends on not only modulation index M (since G is a function of M according to (18)), but also load parameters and inductor resistance.

Fig. 4 shows VTR versus modulation index M for three phase RL load of 60 Ω and 0.3H per phase at 50Hz. In this figure, the effect of r is given for SB, MB and MCB control techniques for the inductor resistance of 2.5Ω. It's obvious that, at low values of modulation index, effect of r increases. This is attributed to high drawn source current which results in high voltage drop.

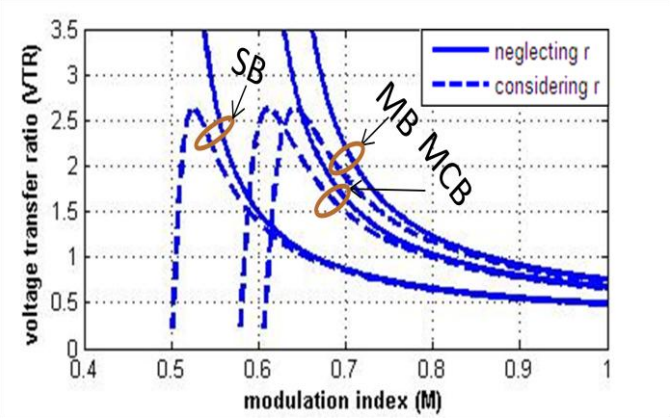


Fig. 4. Voltage transfer ratio versus modulation index considering and neglecting inductor internal resistance "r" where r=2.5Ω

As shown in Fig. 4, VTR increases with decreasing modulation index, until it reaches to the maximum value of M_m. Beyond this point VTR begins to decrease due to high inductor current that causes high voltage drop. At this point:

$$\frac{d\,VTR}{d\,M} = 0 \tag{39}$$

Using (38) and (39), M_m can be obtained to be as follows:

$$M_m = \frac{16n + 4\sqrt{\frac{12r\cos(\Phi)}{Z_L}}}{16n^2 - \frac{12r\cos(\Phi)}{Z_L}} \quad (40)$$

M_m depends on load parameters, inductor resistance and adopted control technique. It is good to operate at modulation index greater than M_m to avoid high operating inductor current.

Fig. 5 shows voltage transfer ratio versus modulation index for different inductor resistance 0, 2, 4 and 6Ω for MCB technique.

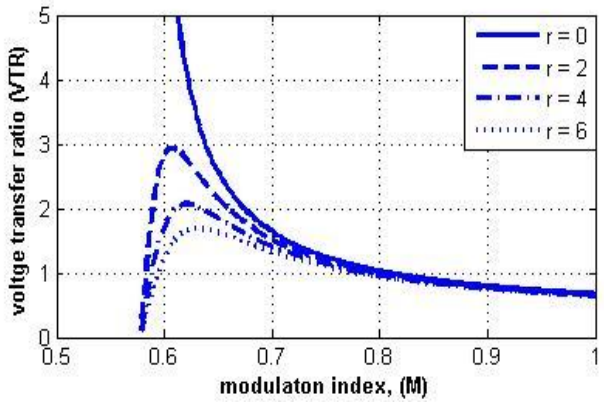


Fig. 5. Voltage transfer ratio versus modulation index for different inductor resistance for MCB control technique

Fig. 6 shows boost factor (V_{dc}/E_s) versus modulation index M when considering inductor resistance (r).

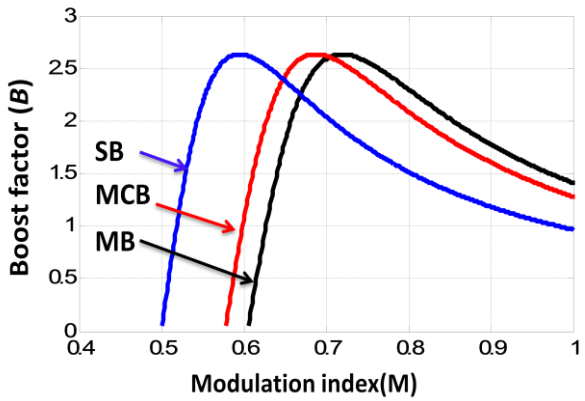


Fig. 6. Boost factor versus modulation index considering and neglecting inductor internal resistance "r"

IV. EXPRIMENTAL RESULTS

To demonstrate the validity of the above analysis for the performance of three-phase ZSI inverter feeding inductive load, simulation and experiments were conducted with the configuration in Fig. 1. Simulation and experimental parameters are:

TABLE II. EXPERMINTAL PARAMETERS

Source voltage (E_s)	20 V	**Load resistance (R_L)**	60Ω
Z-inductance (L_Z)	0.145H	**Load inductance (L)**	0.295H
Z-capacitance (C_Z)	22μf	**Sampling time (T_s)**	25μsec
Output frequency	50Hz	**Carrier frequency (f_c)**	1 kHz

The simulation study has been carried out using SimPowerSystem toolbox provided within MATLAB/SIMULINK package. Capacitors, diode and MOSFETs have been considered as ideal components except the inductors. The simulation results show a complete coincidence with the previous analysis.

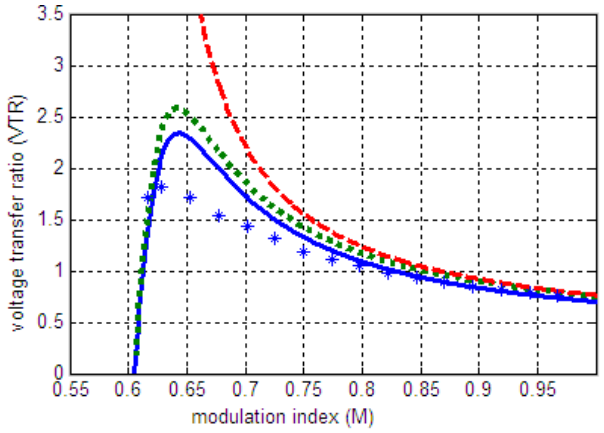
The system was powered from a dc input source at 20V and was driven by a controller using a dSPACE DS1104 card. The employed DSP capabilities limit sampling time to 0.00002 sec. The switching frequency is set to 1 kHz to provide a proper number of samples in the switching cycle.

Fig. 7 and Fig. 8 show voltage transfer ratio VTR versus modulation index M for two control techniques (MB and MCB) that are obtained for two values of inductor resistance 2.5 and 4.5Ω. In both figures, four groups of results are illustrated; namely:

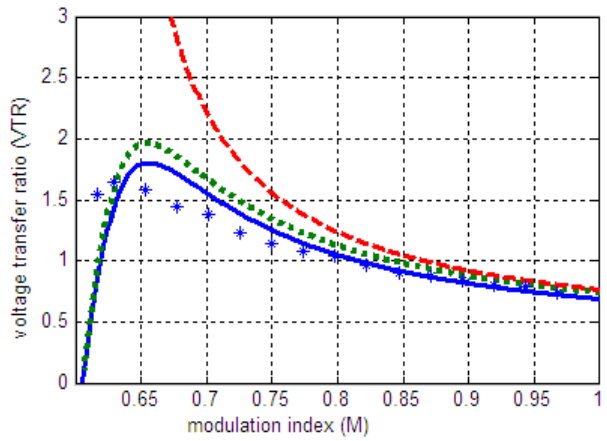
- Neglecting all sources of non-ideality (r, r_{ds}, V_f …etc), (theoretical results)
- Considering only internal resistance of inductor (theoretical results)
- Considering V_f, r and r_{ds} (simulation results)
- Experimental results

According to the given results in Fig. 7 and Fig. 8, the following notes can be extracted:

- At higher values of modulation index, the experimental and theoretical results are well-matched where effects of non-idealities are a little.
- For modulation index M less than about 0.65, there is still discrepancy between experimental and theoretical results are considerable even when V_f, r and r_{ds} are taken into account. This difference may be attributed to:
  1. Assuming inductors and capacitors and resistors are linear, time-invariant, and frequency independent.
  2. The employed DSP capabilities limit sampling time to 0.00002 sec, which may cause losing of some voltage intervals.
  3. Neglecting other types of non-idealities (e.g stray inductances and capacitances) [12].
- It is noted that, value of Mm (maximum VTR) in case of considering r only is very close to that obtained in case of considering r, r_{ds} and V_f.

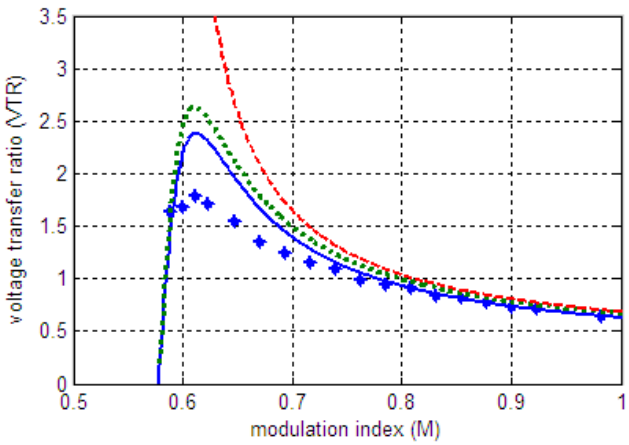


(a)

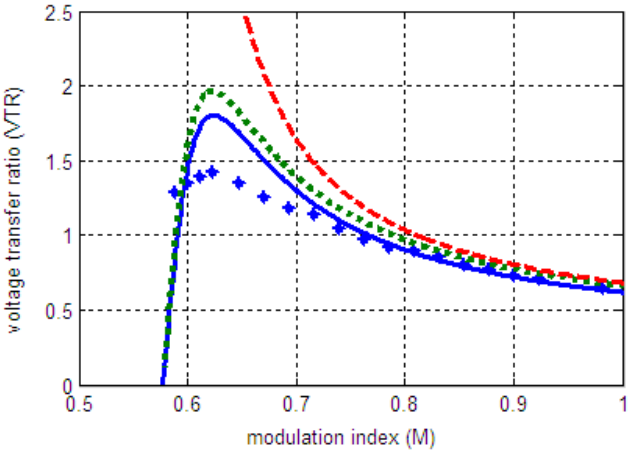


(b)

Fig. 7. Voltage transfer ratio versus modulation index for MB technique



(a) Inductor resistance r=2.5



(b) Inductor resistance r=4.5

Fig. 8. Voltage transfer ratio versus modulation index for MCB technique

Neglecting r, r_{ds} and V_f
Considering r only
Considering r, r_{ds} and V_f
**** Experimental results

- It is not recommended to operate at M less than Mm due to high drawn source current. Moreover, the same VTR can be obtained at values of M greater than Mm with achieving less drawn current.
- Effect of V_f and r_{ds} is low compared with effect of r. Hence, the obtained simple and closed formula for VTR (38) considering r only is sufficient especially when value of r is high compared with r_{ds}.

V. CONCLUSION

A steady-state analysis of Z-source inverter has been presented in details considering inductor parasitic resistance. The output-to input voltage transfer ratio for ZSI has been derived for ideal case and when considering inductor parasitic resistance only. A laboratory prototype and simulink model was built to verify the validity of theoretical analysis. Both simulation and experimental results are in a good agreement with those obtained using the suggested formula for considering inductor internal resistance.

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